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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/587,529	06/01/2000	Yuji Kojima	FUJI 17.379	9500

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EXAMINER	
NGUYEN, QUANG N	

ART UNIT	PAPER NUMBER
2141	

DATE MAILED: 04/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/587,529	KOJIMA ET AL.	
	Examiner	Art Unit	
	Quang N. Nguyen	2141	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 February 2005* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 June 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

Detailed Action

1. This Office Action is in response to the Amendment filed on 02/07/2005. Claims 1 and 8 have been amended. Claims 1-12 are pending for examination.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-2 are rejected under 35 U.S.C. 103(a) as being unpatentable over McMurray et al. (US 4,145,686), herein after referred as McMurray, in view of Toda.

4. As to claim 1, McMurray teaches a packet data processing apparatus for processing a packet received from a network by a processor, comprising:

a packet data access part, which has a plurality of registers arranged in series *(the memory device 28 of Fig. 1 comprised of plurality of serially connected shift registers)*, shifting the received packet through the plurality of registers toward an outlet *(multiplexer 33 or sequencer 41)* in synchronization with a clock *(sequencer 41 provides a clock pulse on line 56 which is synchronized with the pulse on line 38 to shift the data*

through the memory 28 at the same rate as it is generated within the data lift 22) (McMurray, Fig. 1, C4: L11-23);

wherein the processor processes the received packet *(the logic sequencer 41 counts the number of redundancies in a train to determine if a redundancy exists; monitors the stream to locate the primary signals within the data stream and inserts the control markers, redundancy counts, and addresses at their proper locations within the data stream)* while the received packet is being shifted through the plurality of registers, independently of an instruction order for processing the received packet (McMurray, C2: L19-39 and C4: 11-32);

the processor and the packet data access part are directly connected *(the logic sequencer 41 and the memory device 28 are directly connected via channel 52)*;

the processor reads out or writes data from or to the packet data access part by synchronizing the cycle time of the processor *(sequencer 41 provides a clock pulse on line 56 which is synchronized with the pulse on line 38 to shift the data through the memory 28)* (McMurray, Fig. 1 and C4: L11-23).

However, McMurray does not explicitly teach each of the plurality of registers of the packet data access part is connected to a neighbor register via a selector which selects write data from the processor of the neighbor register.

In a related art, Toda teaches two sets of registers to be connected in serial, each consisting of the selector and shift register as illustrated in Fig. 5, wherein the selector performs the selecting operation thereof in response to a data change write signal DC (Toda, Figs 1 and 5, C6: L33-44).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the teachings of McMurray and Toda to connect each of the plurality of registers of the packet data access part to a neighbor register via a selector which selects write data from the processor of the neighbor register since such methods were conventionally employed in the art to provide the system a selecting means for selecting one of plural pieces of information stored in the memories (i.e., registers) to supply to each of the modulation operation systems as the plural pieces of input information (Toda, C2: L12-16).

5. As to claim 2, McMurray-Toda teaches the packet data processing apparatus of claim 1, further comprising:

an intermediate data maintaining part, which has a plurality of registers arranged in series *(the memory device 28 of Fig. 1 comprised of plurality of serially connected shift registers)*, sequentially shifting intermediate data showing a process result of the received packet through the plurality of registers toward the outlet *(multiplexer 33 or sequencer 41)* in synchronization with a clock *(sequencer 41 provides a clock pulse on line 56 which is synchronized with the pulse on line 38 to shift the data through the memory 28 at the same rate as it is generated within the data lift 22)* (McMurray, Fig. 1, C4: L11-23).

6. Claims 3-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over McMurray, in view of Toda, and further in view of Angle et al. (US 6,519,225), herein after referred as Angle.

7. As to claims 3-7, McMurray-Toda teaches the packet data processing apparatus of claim 1, but does not explicitly teach further comprising a search table, wherein said processor searches the search table using data of the received packet, retrieves information corresponding to the data of the received packet and processes the received packet being shifted in accordance with a set of instructions for executing a checksum calculation and a Time-to-Live calculation.

In a related art, Angle teaches a method and apparatus for scheduling multicast data in an input-queued network device, wherein the forwarding logic 106 determines the output port(s) to which received packets need to be forwarded and performs other Internet Protocol (IP) header processing, such as appending the next hop Media Access Control (MAC) address *(as well-known in the art, the MAC address is a 48-bit field that includes addresses for both source addresses and destination addresses that can be unicast, multicast or broadcast addresses)* retrieved from a forwarding data base *(i.e., a search table)*, updating the Time-to-Live (TLL) field, and calculating a new header checksum (Angle, C4: L20-26).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the teachings of McMurray-Toda and Angle to include the steps of searching the search table to retrieve information corresponding

to the data of the received packet and processing the received packet with a set of instructions for executing a checksum and Time-to-Live calculation because it were conventionally employed in the art to allow the system to identify the destination address in the received packet, retrieve the transmission information *(from the forwarding database, i.e., search table)* and calculate the header error checksum to determine how and whether to route the information received to the destinations or applications for which they are intended.

8. Claims 8-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over McMurray-Toda, in view of Klim et al. (US 6,519,225), herein after referred as Klim.

9. As to claims 8-10, McMurray-Toda teaches the packet data processing apparatus of claim 1, but does not explicitly teach a plurality of processors being connected in series in that packet sequentially passes through the plurality of processors in stead of plurality of registers connected in series.

In a related art, Klim teaches a data processing apparatus that has a number of data processors connected in a series by data lines so that data signals are processed in a preceding processor and communicated to a succeeding processor in the series, comprising:

a plurality of processors being connected in series (Pa, Pb, Pc and Pd of Fig. 3), wherein each processor receives and processes data, holds the processed data, and

then sends the data to the next processor in the pipeline or to a receiving device at the end of the pipeline (Klim, C4: L34-37).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the teachings of McMurray and Klim to have a plurality of processors being connected in series in that the received data packet is sequentially shifted and processed through the plurality of processors since such methods were conventionally employed in the art to process data in stages where the processing result of one state is passed to a subsequent stage for further processing by succeeding processors *(pipeline processors)* in the series or to have a series of interconnected processing stages, where the stages may operate concurrently to improve the processing data at a very high speed in a series of processors environment.

10. Claims 11-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over McMurray-Toda, in view of Donley (US 6,081,538).

11. As to claims 11-12, McMurray teaches the packet data processing apparatus of claim 1, but does not explicitly teach further comprising a write/read-position changing part changing a write/read-position of said plurality of registers of the packet data access part where the write/read-position defines an inlet/outlet point at which said packet data access part receives/sends the packet from/to an exterior thereof.

In a related art, Donley teaches a network node for receiving a packet of data written from the network and providing the packet to the network including a first counter that produces a write-point signal to select a first one of the registers to receive the first data from the network (i.e., to define an inlet point at which said packet data access part receives the packet from an exterior thereof) and a second counter that produces a read-point signal with a further register being selected by the read-point signal to provide the second data to the network (i.e., to define an outlet point at which said packet data access part sends the packet to an exterior thereof) (Donley, Abstract, C3: L38-67 and C4: L1-36).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the teachings of McMurray and Donley to include a write/read-position changing part changing a write/read-position of said plurality of registers of the packet data access part where the write/read-position defines an inlet/outlet point at which said packet data access part receives/sends the packet from/to an exterior thereof because it were conventionally employed in the art to allow the system to synchronize the control signals and data signals with the clock signals to configure the input/output data signals for receiving (inputting) and delivering (outputting) the data to the appropriate destinations.

12. Applicant's arguments as well as request for reconsideration filed on 02/07/2005 have been fully considered but they are moot in view of the new ground(s) of rejection.

13. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

14. Further references of interest are cited on Form PTO-892, which is an attachment to this office action.

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quang N. Nguyen whose telephone number is (571) 272-3886.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's SPE, Rupal Dharia, can be reached at (571) 272-3880. The fax phone number for the organization is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Quang N. Nguyen

RUPAL DHARIA
SUPERVISORY PATENT EXAMINER